



Perfect Signal Integrity in the High-Speed Age

Optimization of High-Speed Plug Connectors



How does HighSpeed affect developers?

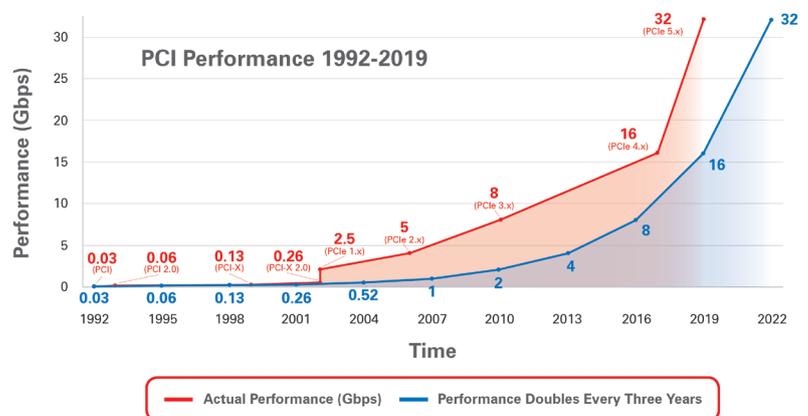
The wave properties of a high-frequency signal mean that developers of digital circuits are increasingly encountering influences familiar from the analog era. High-performance imaging applications and 5G mobile communications require a unified understanding of the influencing and evaluation criteria for high-speed performance. The signal integrity benefits from the most uniform impedance curve possible along the transmission path. In early phases of development, this can be achieved by optimizing the connector based on the application conditions. However, existing connectors should also be checked at the fastest required rise time. Since the impedance profile always depends on the frequency spectrum used, a connector with a nominally different impedance may also prove to be optimal.

What is High-Speed?

There is no general answer to this question. Rather, high-speed must be viewed relatively. This can be demonstrated through the example of the development of the PCI Express specification, or PCIe for short.

Fig. 1:

Historical development of the PCI, PCI-X, and PCI Express specification since 1992.
Illustration: ept GmbH



The change from Gen 4 (16 Gbps) to Gen 5 (32 Gbps) has only just occurred, and work has already started on the specification for Gen 6 with 64 Gbps. In terms of application requirements, each PCI/PCIe generation was considered the current high-speed variant at its time. However, the discrepancy between 3 Mbps PCI in 1992 and 32 Gbps PCIe 5.x in 2019 is enormous.

This results in continuously increasing demands on the input and processing power of connectors.

Maintaining signal integrity is an ever-increasing challenge. What was previously only a problem for high-frequency developers is now encountered by hardware developers of digital circuits due to modern data rates:

During analog times, data transfer rates were optimized with great care and precision to avoid interference; all the while, the seemingly infinite potential of digital transmission was exploited extensively using less layout effort. Much like the semiconductor industry, which constantly had to overcome “apparent” physical limits and then rely on innovation, digital transmission is also increasingly experiencing problems. As a result, more and more signal disturbances particularly known from the long-gone analog era gain relevance again at ever higher data transfer rates. It must be noted here that each digital signal has been generated from an analog source. The interpretation of the electrical signal as an electromagnetic wave suggests that the influences from the analog era are becoming more relevant again with increasing performance demands.

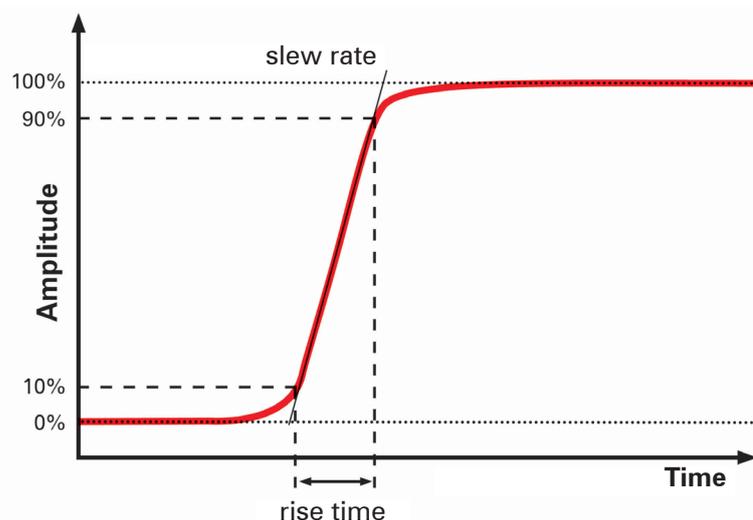
Rise time – state change of digital signals

At a time when data exchange and data transfer rates in applications such as imaging and 5G mobile communications are increasing, it is extremely important that both connector manufacturers and users understand the influence and evaluation criteria of high-speed performance.

The so-called “rise time” is one way of getting closer to “high-speed.” It refers to the time required by a logical system to change its state.

Fig. 2:

The logical state of a signal changes during the rise time.
Illustration: ept GmbH



Digital systems ideally run on rectangular signals, which can change their state instantaneously. In reality, however, changing states takes time. Rise time is the time in which the signal lies between two defined amplitude values (usually 10 percent and 90 percent). The lower the rise time, the larger the bandwidth.

Which plug connector...

is right for which applications?

This question can be partially answered with the performance data by plug connector manufacturers. But the specifications are not straightforward. Some manufacturers provide specifications in the analog frequency spectrum (GHz), while others use the digital data transfer rate (Gbps). Both values are usually determined using insertion loss measurements.

More often than not, the frequency range is used until an insertion loss of -3dB is reached. This is where the relevant cut-off frequency lies. In a signal with two logical states per amplitude, the data transfer rate is obtained by doubling the cut-off frequency.

Pay attention to customer requirements

For new developments without target specifications, it is critical for the plug connector manufacturers to work closely with the customer. The better the operating conditions and requirements are known, the easier it is to attune the connector.

The most important information is how much space is available on the module, connector design ideas, the desired connection technology, the number of pins, and the pin assignment, as well as the performance requirements.

Plug connector optimization

One of the challenges of designing high-speed plug connectors is to control their impedance. This is determined by inductive and capacitive characteristics, which in turn depend upon the size, arrangement, and design of the pins, among other things. The introduction of dielectrics into the connector must also be carefully evaluated, as these can influence the signal integrity through the effect of signal propagation.

The following formula is used to calculate the impedance:

$$Z = \sqrt{L/C}$$

Z = Impedance

L = Inductivity

C = Capacitance

It must be observed that the impedance changes along the signal path of the plug connector dependent on changes in geometry and cross-section.

This means that there are various factors to consider in the control of impedance.

A decrease in impedance is achieved by reducing the inductive share or by increasing the capacitive share in the connector.

Thicker signal pins are a common example. Higher impedance is achieved by carrying out the opposite steps. This can be realized by increasing the pin distance. The insulator material affects the capacitance, as the dielectric conductivity (permeability of a material) is tied to the capacitance. A higher dielectric value lowers impedance.

Improperly adjusted impedance can result in some of the signals being reflected, so they do not reach their target.

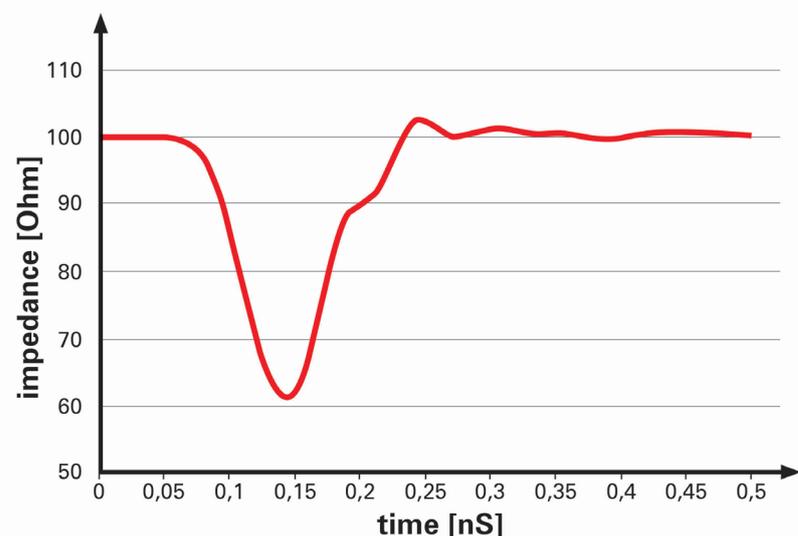
How is impedance measured?

Impedances are determined using Time Domain Reflectometry (TDR). This allows the signal transmission environment to be viewed over a time domain by detecting run lengths and reflections of electrical signals.

A pulse is injected into the signal path for this purpose. As long as the medium does not change, the wave impedance remains the same along the signal path. Any change to the cross-section or material results in impedance changes. This creates reflections that are reflected back along the signal path. The strength and arrival time of the reflections make it possible to draw conclusions about the respective impedance along the signal path.

Fig. 3:

Example impedance curve of the Colibri plug connector from ept. Illustration: ept GmbH



Optimizing a connector for a particular impedance profile does not mean that it cannot be used in any other environment. The impedance profile of a signal chain or connector is always the result of the interaction of the previously defined influences (cross-sectional change, material changes) and the applied signal. The longer the rise time, the smaller the associated influences and the closer the impedance is to that of the rest of the system. This is especially important for the user, since a plug connector

with an impedance suitable for the system does not necessarily have to be used. It is also much more important to determine the fastest rise time for the system application and evaluate the corresponding impedance of the plug connector.

As previously described, impedance deviations result in signal reflections. This can mainly be noticed in the form of insertion loss and return loss.

Insertion loss describes the loss of signal or power along the signal path as the ratio of outgoing to incoming signal. The insertion loss consists of different components, including coupling losses, dielectric losses, reflection losses, conductor losses, and radiation losses that need to be considered.

Return loss is the portion of the reflected signal in the inserted signal. It is important here that the entire signal path must be considered when considering the return loss, since this tends to decrease with the length of the signal path.

Evaluation of signal quality using an eye diagram

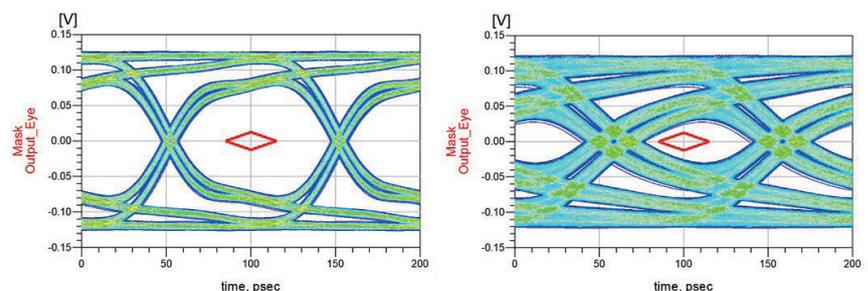
A visual evaluation of a signal's "legibility" can be carried out using the "eye diagram." This illustrates whether a transmitted signal in the receiver can be uniquely assigned to the digital states 1 or 0.

A signal passes through a defined transmission path, is recorded with an oscilloscope, superimposed, and displayed. This allows all possible signal characteristics to be displayed "on top of each other." According to theory, the transitions of the logical states are infinitely steep and the signal lines are precisely superimposed. The reality is different. Signal influences and interference flatten the signal rise while the amplitude level changes.

This results in the shape of an eye that gives the diagram its name.

Fig. 4:

The eye diagram is used to evaluate the signal quality of a digital data transfer rate.
Illustration: ept GmbH



The area in the middle of the diagram represents the "eye mask." A signal cannot be uniquely assigned in this area.

The width of the “eye” indicates the possible time period for scanning the signal, which is limited by jitter and symbol crosstalk.

Both eye diagrams illustrate the influences of cable length and impedance using the ept Colibri plug connector as an example. While the first eye is shaped nicely by a short line length and 100 Ω impedance, the second eye reveals a worse signal quality through a higher line length and different impedances on both boards (100 Ω and 110 Ω).

An optimized connector is only possible if you have exact customer requirements

The various influencing criteria, stress fields, and dependencies complicate the planning of new high-speed plug connectors. For this reason, lots of effort is invested in the evaluation of the exact requirements (including in cooperation with customers) and in the simulation of possible designs in early development phases. Knowing the requirements more precisely means that the connector can be optimized in a more targeted manner. Pinouts defined for many transmission standards provide great help for this. Already included ground channels assist in reducing crosstalk without, for example, increasing the pin spacing too much.

The plug connector manufacturer generates the scattering parameters (S-parameters) from its 3D data and thereby captures the development progress. Typically, customers will receive the S-parameters of the end product so they can simulate their own design. Ideally, the S-parameters should only include the behavior of the connector, since all other influencing parameters are defined by the user.

Simulations allow for a relatively precise analysis of the later behavior of the plug connectors as well as the verification of the plug connectors' sensitivity to the environmental conditions. This means that the first development iterations occur before the order of prototype tools is placed.

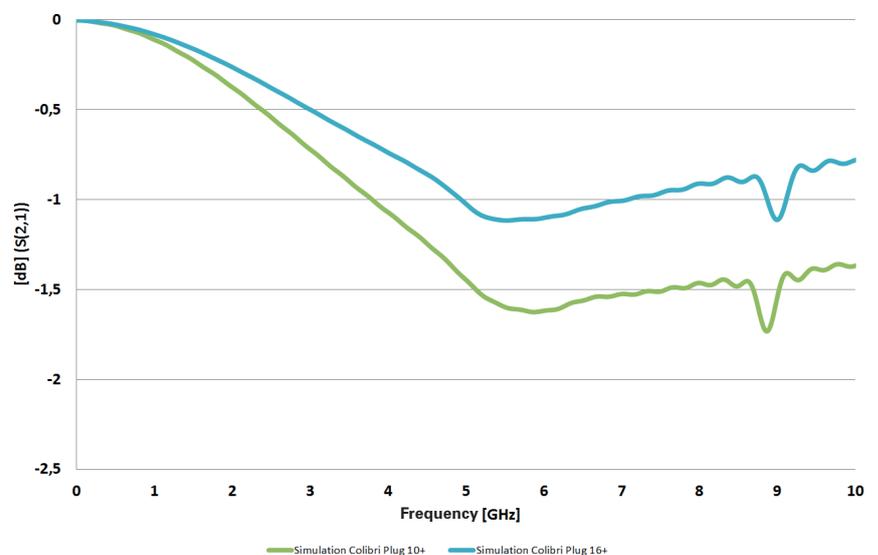
A current example:

the Colibri 16+ high-speed SMT PCB connector

Ingenious optimizations in the contact design of the plug connectors were responsible for the releases of the 10+ Gbps version (and since the end of 2018, the 16+ Gbps version), while maintaining plug compatibility at all times. Since 2020, the 40–160 pin versions of the proven COM-Express connector have also been available as 16+ versions. The illustration below shows a significant improvement in the insertion loss of the Colibri connector for 16+ Gbps applications.

Fig. 5:

Optimization of ept Colibri plug connectors from 10+ Gbps to 16+ Gbps. Illustration: ept GmbH



Optimizing the contact design of the plug achieved an improvement of up to 35 percent. The Colibri Plug 16+ thus offers excellent data transfer rates for USB 3.1 Gen2 and PCI Express 4.0 signals. This shows how great the influence of each individual element can be in the interaction of the plug connector.

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Further information can be found here: www.ept.de/Colibri

You can watch the unboxing video of our Colibri connector here: <https://youtu.be/VHc3bHVIGHc>